PRODUCT BRIEF

Z80230

ESCC™ ENHANCED
SERIAL COMMUNICATION CONTROLLER

FEATURES

- Deeper Data FIFOs
  - 4-Byte Transmit FIFO
  - 8-Byte Receive FIFO
- Programmable FIFO Interrupt Levels Provide Flexible Interrupt Response
- Pin and Function Compatible to CMOS and NMOS Z80C30 SCC
- Many Improvements to Support SDLC/HDLC Transfers:
  - Deactivation of /RTS Pin after Closing Flag
  - Automatic Transmission of the Opening Flag
  - Automatic Reset of Tx Underrun/EOM Latch
  - Complete CRC Reception
  - TxD Pin Automatically Forced High with NRZI Encoding when Using Mark Idle.
  - Receive FIFO Automatically Unlocked for Special Receive Interrupts when Using the SDLC Status FIFO.
  - Back-to-Back Frame Transmission Simplified
- Easier Interface to Popular CPUs
- Fast Speeds:
  - 10.0 MHz for Data Rates up to 2.5 Mbit/sec.
  - 16.384 MHz for Data Rates up to 4.096 Mbit/sec.
- Improved SDLC Frame Status FIFO
- Low Power CMOS
- New Programmable Features Added with Write Register 7'
- Write Registers: WR3, WR4, WR5, and WR10 are Now Readable
- Read Register 0 Latched During Access
- Software Interrupt Acknowledge Mode
- DPLL Counter Output Available as Jitter-Free Clock Source
- /DTR//REQ Pin Deactivation Time Reduced
- Two Independent Full-Duplex Channels, Each with a Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop.
- Multi-Protocol Operation under Program Control
- Asynchronous Mode with Five to Eight Bits, and One, One-and-One-Half, or Two Stop Bits per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with Programmable CRC Preset Values.

GENERAL DESCRIPTION

The Zilog Enhanced Serial Communications Controller, Z80230 ESCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. The ESCC is a dual-channel, full-duplex data communications controller capable of supporting a wide range of popular protocols. The ESCC is built from Zilog's industry standard SCC core and is compatible with designs using Zilog's SCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitters and receivers.

The ESCC also has many features that improve packet handling in SDLC mode. The ESCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the

GENERAL DESCRIPTION *(Continued)*

closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the ESCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

The many enhancements added to the ESCC permits a system design that increases overall system performance with better data handling and less interface logic.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

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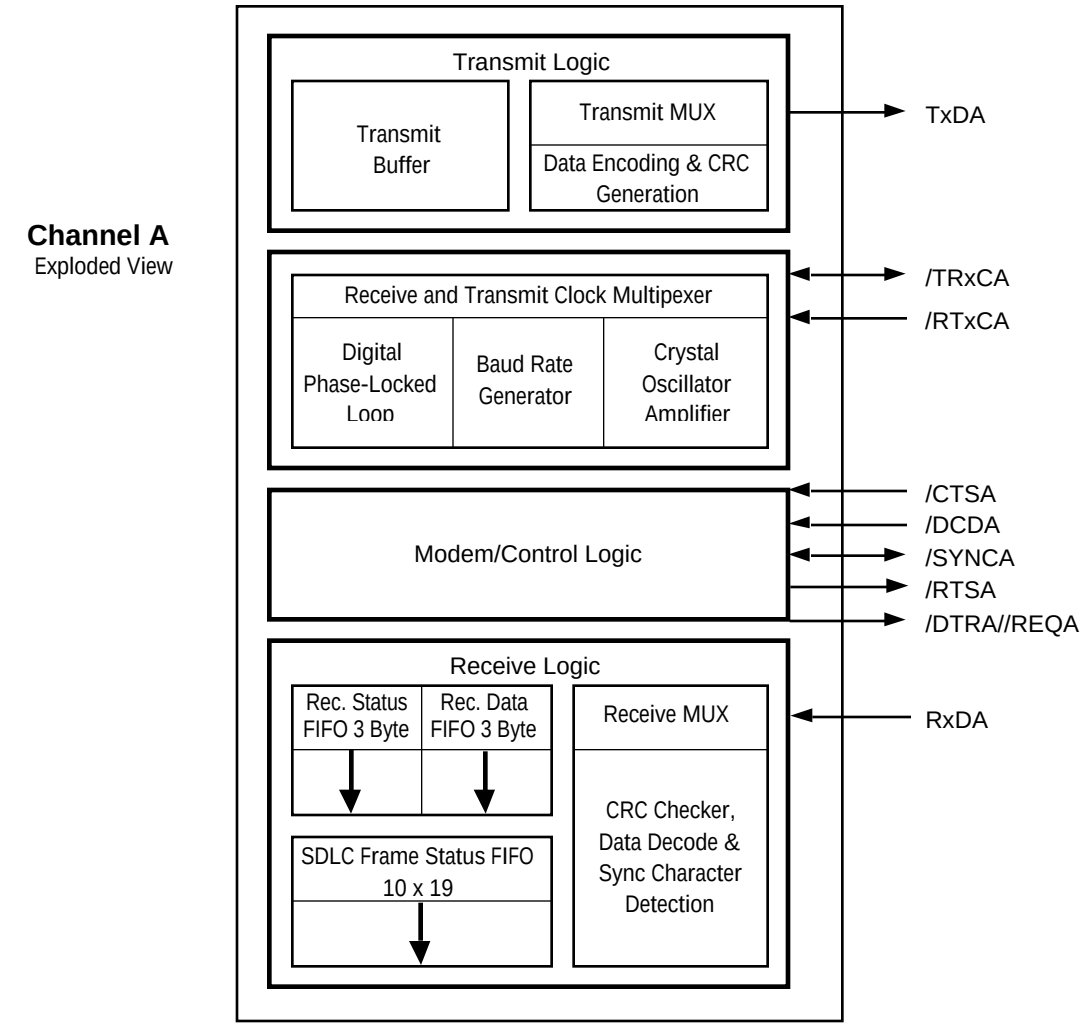

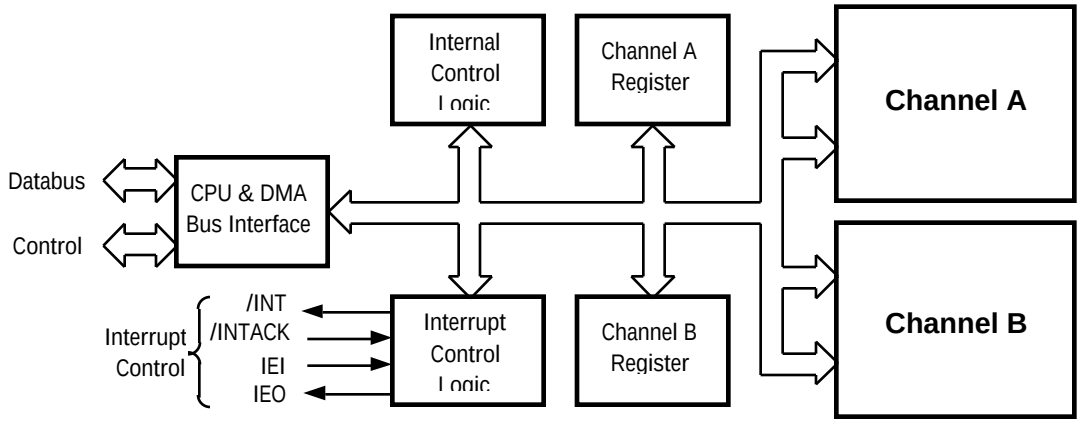

Z80230 Functional Block Diagram